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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,779	12/22/2000	Hong Koo Kim	000939073311	4408

20350 7590 10/21/2003

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 10/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,779	KIM, HONG KOO	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,23,24 and 26-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,23,24 and 26-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: 00939-073311 US

Filing Date: 12/22/2000

Claimed Priority Dates: 3/29/2000 (Provisional 60/193,046)
12/27/1999 (Provisional 60/173,175)

Applicant(s): Kim

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 16 filed on 7/28/2003.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after the final rejection in paper no. 11, mailed on 2/25/2003. Since this application is eligible for a continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/28/2003 has been entered.

Acknowledgments

2. The amendment in paper no. 16, filed on 7/28/2003, in response to the Office action in paper no. 11, mailed on 2/25/2003, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-21, 23, 24, and 26-34.

3. The declaration under 37 CFR 1.132 in paper no. 15, filed on 7/28/2003, has been entered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 28 and 30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

6. Claims 28 and 30 recite that the MgO layer had a polycrystalline or a highly oriented structure prior to the annealing step. The description in the original disclosure fails to support this limitation in the claims. The original description does teach that highly oriented MgO layers have a polycrystalline structure (see, *e.g.*, pp.7/ll.15-20). It also describes that thin MgO layers are more likely to have an amorphous structure (see, *e.g.*, pp.7/ll.15-20). Nowhere in the original disclosure, however, it is specified that prior to the annealing step the MgO layer had a polycrystalline structure or that it was deposited as a highly oriented layer.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 21, 23, 24, and 26-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Lines 8 and 9 of claim 21 recite the limitation "the second buffer layer". There is insufficient antecedent basis for this limitation in the claim.

10. Line 1 of claim 24 recites the limitation "the second buffer layer". There is insufficient antecedent basis for this limitation in the claim.

11. Line 1 of claim 26 recites the limitation "the second buffer layer". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1, 3-10, 14-18, 20, 21, 23, 24, and 27 are rejected under section 35 U.S.C. 103(a) as being unpatentable over Hirai (US 5955755), Kirlin (US 5225561), Maiti (US 6020024), and Iyer (US 5629246).

14. Regarding claim 1, Hirai shows (see, *e.g.*, figs. 1, 2D, 2E, 3A, and 3B) most aspects of the instant invention including a method for fabricating a non-volatile memory device, the method comprising:

- providing a substrate **1**
- forming an oxide layer **4** overlying the substrate **1**
- forming a buffer layer **5** on the oxide layer **4** after forming the oxide layer **4** over the substrate **1**
- forming a ferroelectric material **6** overlying the substrate **1**

- forming a gate layer **7** overlying the ferroelectric material **6** and a channel region
- forming a first source/drain region **2** adjacent to a first side of the channel region
- forming a second source/drain region **3** adjacent to a second side of the channel region

Hirai, however, fails to show a step of thermally annealing the buffer layer. Nonetheless, annealing steps are thermal treatments commonly used in the semiconductor art to eliminate various weaknesses, or to produce other qualities in a material. As taught by Kirlin (see, *e.g.*, col.35/ll.30-33) and Maiti (see, *e.g.*, col.3/ll.33-36 and col.4/ll.10-14), such an annealing step will remove the vacancies of Hirai's buffer layer, thereby improving its quality and reducing its defects.

It would have been obvious at the time of the invention to one of ordinary skill in the art to include in Hirai's method a step of thermally annealing the buffer layer, as suggested by Kirlin and Maiti, to improve the quality of the layer.

Hirai also fails to teach that the oxide layer has an amorphous surface structure. Nonetheless, Hirai (see, *e.g.*, col.7/ll.38) shows that the first buffer layer is a silicon-dioxide layer, which is used as a dielectric. As taught by Iyer (see, *e.g.*, col.1/ll.16-20), silicon dioxides used as dielectrics in integrated circuits are typically amorphous materials.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time of the invention that Hirai's oxide layer is amorphous,

as taught by Iyer, since this is a silicon dioxide layer used as a dielectric and silicon dioxides used as dielectrics in integrated circuits are typically amorphous.

15. Regarding claim 3, Hirai shows that the ferroelectric material may be a PZT-bearing compound (see, *e.g.*, col.2/ll.40-43).

16. Regarding claim 4, Hirai shows that the buffer layer may be a magnesium-bearing compound (see, *e.g.*, col.2/ll.39).

17. Regarding claim 5, Hirai shows that the buffer layer may be a magnesium-oxide layer, the magnesium-oxide layer being a barrier layer (see, *e.g.*, col.2/ll.39, col.3/ll.7-10, col.4/ll.62-67).

18. Regarding claim 6, Hirai shows that the ferroelectric material may have a thickness of less than about 1000 angstroms (see, *e.g.*, col.4/ll.42).

19. Regarding claim 7, Hirai shows that the buffer layer may have a thickness of 20 nanometers (see, *e.g.*, col.4/ll.13-14).

20. Regarding claim 8, Hirai shows that the ferroelectric material may have a thickness greater than 100 angstroms (see, *e.g.*, col.4/ll.42).

21. Regarding claim 9, Hirai shows that the ferroelectric material may be PZT (see, *e.g.*, col.4/ll.37).

22. Regarding claim 10, Hirai shows that the buffer layer is a diffusion barrier layer substantially preventing the diffusion between the ferroelectric material and the substrate (see, *e.g.*, col.4/ll.62-67).

23. Regarding claim 14, Hirai shows that the ferroelectric material is highly oriented (see, *e.g.*, col.4/ll.40-41, col.5/ll.48-52).

24. Regarding claims 15 and 16, Hirai (see, *e.g.*, col.10/ll.17-18) shows that the ferroelectric material is a highly oriented (001) thin film. The polycrystallinity of Hirai's highly oriented ferroelectric material is an inherent property. Hirai, for example, shows that his ferroelectric material is a highly oriented PZT thin-film showing a (001)-face (see, *e.g.*, col.4/ll.50-52). (001)-PZT planes are polycrystalline (see remarks section below).

25. Regarding claim 17, Hirai shows that the polycrystalline film is greater than 100 angstroms (see, *e.g.*, col.4/ll.42).

26. Regarding claim 18, Hirai shows that the buffer layer is a template to provide an oriented growth of the ferroelectric film (see, *e.g.*, col.4/ll.31-35)

27. Regarding claim 20, Hirai shows that the oxide layer is silicon dioxide (see, *e.g.*, col.9/ll.58). The substrate-surface passivation-property is inherent to Hirai's oxide layer (see remarks section below).

28. Regarding claim 21, Hirai shows (see, *e.g.*, figs. 1, 2D, 2E, 3A, and 3B) most aspects of the instant invention including a method for fabricating a non-volatile memory device, the method comprising:

- providing a semiconductor substrate **1**
- forming a gate oxide layer **4** on the substrate **1**
- forming a MgO layer **5** overlying the oxide layer **4** after forming the oxide layer **4** on the substrate **1**
- forming a ferroelectric material **6** overlying the substrate **1**

- forming a gate layer **7** overlying the ferroelectric material **6** and a channel region
- forming first and second doped regions **2, 3** adjacent to first and second ends of the channel region

Hirai, however, fails to show a step of thermally annealing the buffer layer. Nonetheless, annealing steps are thermal treatments commonly used in the semiconductor art to eliminate various weaknesses, or to produce other qualities in a material. For example, Kirlin (see, *e.g.*, col.35/ll.30-33) and Maiti (see, *e.g.*, col.3/ll.33-36 and col.4/ll.10-14) teaches that thermally annealing Hirai's buffer layer will remove the vacancies of the layer, thereby improving its quality and reducing its defects.

It would have been obvious at the time of the invention to one of ordinary skill in the art to include in Hirai's method a step of thermally annealing the buffer layer, as suggested by Kirlin and Maiti, to improve the quality of the layer.

Hirai also fails to teach that the oxide layer has a non-crystalline structure. Nonetheless, Hirai (see, *e.g.*, col.7/ll.38) shows that the first buffer layer is a silicon-dioxide layer, which is used as a dielectric. As taught by Iyer (see, *e.g.*, col.1/ll.16-20), silicon dioxides used as dielectrics in integrated circuits are typically amorphous materials.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time of the invention that Hirai's oxide layer is amorphous since, as taught by Iyer, this is a silicon dioxide layer used as a dielectric and silicon dioxide layers used as dielectrics in integrated circuits are typically amorphous.

29. Regarding claim 23, Hirai (see, *e.g.*, col.4/ll.49) shows that the MgO layer is a highly oriented layer, whereas Iyer (see, *e.g.*, col.1/ll.16-20) shows that the oxide layer is amorphous.

30. Regarding claim 24, although Hirai does not show the MgO layer has a thickness of less than 10 nm, he shows that his paraelectric oxide thin layer may be approximately 14 nm (see, *e.g.*, col.12/ll.3). Hirai's thickness appears to be closed enough to the claimed thickness range that one of ordinary skill in the art would have expected Hirai's MgO layer to have the same properties as those of the claimed layer; consequently, it would have been obvious. *Titanium Metal Corp. of America v. Banner*, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985).

Moreover, it would be an obvious matter of design choice to have a thickness not greater than 10 nm, instead of 14 nm, for Hirai's MgO layer since such a modification would have involved a mere change in the size of the layer. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

31. Regarding claim 27, Hirai shows that the MgO layer has a highly oriented structure.

32. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Iyer in view of Yamazaki (US 6072724).

33. Regarding claim 2, Hirai/Kirlin/Maiti/Iyer shows most aspects of the instant invention (see paragraphs 14-31 above) but fails to specify the channel region to be about 1 micron or less.

Yamazaki (see, *e.g.*, col.2/ll.45-46), on the other hand, teaches that it is known that the channel length is an important design parameter that will determine the channel current of the transistor.

Consequently, it would be an obvious matter of design choice to select a suitable channel length for the transistor of Hirai/Kirlin/Maiti/Iyer, as suggested by Yamazaki, since the channel length is a variable of importance subject to routine experimentation and optimization and it is not inventive to discover the optimum or workable ranges by routine experimentation.

34. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Iyer in view of Van Zant and Evetts (US 5361720).

35. Regarding claim 11, Hirai/Kirlin/Maiti/Iyer shows most aspects of the instant invention (see paragraphs 14-31 above), except for sputtering the buffer material from a substantially pure magnesium target to form a magnesium oxide layer. Hirai differently deposits the magnesium layer using vacuum evaporation (see, *e.g.*, col.4/ll.10-12).

Van Zant (pp.412), however, teaches that there are several advantages to the use of sputtering over vacuum evaporation. One is the improvement in step coverage. Evetts (see, *e.g.*, col.2/ll.15-20), on the other hand, teaches that sputter deposition from a magnesium metal target in a sputtering gas comprising oxygen is a preferred method of forming a high-quality MgO layer.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to sputter Hirai/Kirlin/Maiti/Iyer's buffer layer from a magnesium

target to form the MgO layer, as suggested by Van Zant and Evetts, in order to improve the step coverage while forming a high-quality MgO layer.

36. Regarding claim 12, Hirai shows most aspects of the instant invention (see paragraph 14-31 above). In addition, Evetts (see, *e.g.*, col.2/ll.2) shows that the deposition temperature may be as low as 540°C. Hirai/Kirlin/Maiti/Iyer/Van Zant/Evetts, however, fails to teach a sputtering temperature between 400-500°C.

In spite of the above, generally, differences in temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

There is no evidence supporting the claimed temperature range, *i.e.*, 400-500°C, as critical to the invention, and therefore it would have been obvious.

37. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Iyer/Van Zant/Evetts and Wolf.

38. Hirai/Kirlin/Maiti/Iyer/Van Zant/Evetts shows most aspects of the instant invention (see paragraphs 35 and 36 above). In addition, Kirlin (see, *e.g.*, col.35/ll.30-35) shows that the annealing step may be performed at 700°C for 20 minutes. Hirai/Kirlin/Maiti/Iyer/Van Zant/Evetts, however, fails to perform the annealing between 800-1000°C for about 30 minutes.

Wolf (pp.57), on the other hand, teaches that it is known that temperature and time are important design parameters affecting wafer warpage or slip and dopant diffusion.

Consequently, it would be an obvious matter of design choice to select a suitable temperature and time for the anneal step of Hirai/Kirlin/Maiti/Iyer/Van Zant/Evetts, as taught by Wolf, since these are variables of importance subject to routine experimentation and optimization and it is not inventive to discover the optimum or workable ranges by routine experimentation.

In spite of the above, generally, differences in temperature and time will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

There is no evidence supporting the claimed temperature range and time value, as critical to the invention, and therefore they would have been obvious.

39. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Iyer in view of Jaeger.

40. Regarding claim 19, Hirai/Kirlin/Maiti/Iyer shows most aspects of the instant invention (see paragraphs 14-31 above). Hirai (see, *e.g.*, col.8/ll.2) also teaches that the oxide layer is formed by a thermal oxidation step. He, however, fails to teach the use of a dry oxidation process to form the oxide layer. Jaeger (see, *e.g.*, pp.42), on the

other hand, teaches that dry oxidation would have been commonly used as the thermal oxidation step of Hirai to maintain good process control.

It would have been obvious at the time of the invention to one of ordinary skill in the art to use dry oxidation as the thermal oxidation step in Hirai's method, as suggested by Jaeger, to maintain good process control.

41. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Kirlin/Maiti/Iyer in view of Wolf.

42. Regarding claim 26, see the comments stated above in paragraph 38 with respect to claim 13, which are considered repeated here.

43. Claims 29 and 31-33 are rejected under section 35 U.S.C. 103(a) as being unpatentable over Hirai and Iyer.

44. Regarding claim 29, Hirai shows (see, *e.g.*, figs. 1, 2D, 2E, 3A, and 3B) most aspects of the instant invention including a method for fabricating a non-volatile memory device, the method comprising:

- providing a semiconductor substrate **1**
- forming an oxide layer **4** on the substrate **1**
- forming a highly oriented MgO layer **5** on the oxide layer **4**
- forming a ferroelectric material **6** overlying the substrate **1**
- forming a gate layer **7** overlying the ferroelectric material **6** and a channel region
- forming first and second doped regions **2, 3** adjacent to the first and second ends of the channel region

Hirai, however, fails to disclose that the oxide layer has a non-crystalline structure. Nonetheless, Hirai (see, *e.g.*, col.7/ll.38) shows that the first buffer layer is a silicon-dioxide layer used as a dielectric in a memory device. As taught by Iyer (see, *e.g.*, col.1/ll.16-20), silicon dioxides used as dielectrics in integrated circuits are typically amorphous materials.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time of the invention that Hirai's oxide layer is amorphous, as taught by Iyer, since this is a silicon dioxide layer used as a dielectric and silicon dioxides used as dielectrics in integrated circuits are typically amorphous.

45. Regarding claim 31, Hirai shows (see, *e.g.*, figs. 3A and 3B) that the MgO layer **5** is formed after the oxide layer **4** is formed.

46. Regarding claim 32, Hirai shows (see, *e.g.*, figs. 1, 2D, 2E, 3A, and 3B) most aspects of the instant invention including a method for fabricating a non-volatile memory device, the method comprising:

- providing a semiconductor substrate **1**
- forming a gate dielectric layer **4** on the substrate **1**
- forming an MgO layer **5** on the dielectric layer **4** after forming the dielectric layer **4** on the substrate **1**, the MgO layer **5** having a highly-oriented structure
- forming a ferroelectric layer **6** overlying the MgO layer **5** (see, *e.g.*, col.3/ll.53-col.4/ll.12)

wherein the dielectric layer **4**, the MgO layer **5**, and the ferroelectric layer **6** are patterned to form a transistor.

Hirai, however, fails to disclose that the gate dielectric layer is amorphous. Nonetheless, Hirai (see, *e.g.*, col.7/ll.38) shows that the gate dielectric layer is a silicon-dioxide layer used as a gate dielectric in a memory device. As taught by Iyer (see, *e.g.*, col.1/ll.16-20), silicon dioxides used as dielectrics in integrated circuits are typically amorphous materials.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time of the invention that Hirai's gate dielectric layer is amorphous, as taught by Iyer, since this is a silicon dioxide layer used as a dielectric and silicon dioxides used as dielectrics in integrated circuits are typically amorphous.

47. Regarding claim 33, Hirai shows that the MgO layer has a crystalline structure (see, *e.g.*, col.3/ll.53-col.4/ll.12).

48. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Iyer in view of Kirlin and Maiti.

49. Regarding claim 30, Hirai/Iyer shows most aspects of the instant invention (see paragraphs 44-47 above), except for the step of thermally annealing the MgO layer. Nonetheless, annealing steps are thermal treatments commonly used in the semiconductor art to eliminate various weaknesses, or to produce other qualities in a material. For example, Maiti (see, *e.g.*, col.3/ll.33-36 and col.4/ll.10-14) teaches that annealing Hirai's MgO layer will remove the vacancies of the layer, thereby improving its quality and reducing its defects. Likewise, Kirlin (see, *e.g.*, col.35/ll.7,30-33) teaches that annealing a highly oriented MgO layer eliminates oxygen anion vacancies within the layer.

It would have been obvious at the time of the invention to one of ordinary skill in the art to include in Hirai/Iyer's method a step of thermally annealing the MgO layer, as suggested by Kirlin and Maiti, to improve the quality of the layer.

50. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai/Iyer in view of applicant's admitter prior art.

51. Regarding claim 34, Hirai/Iyer shows most aspects of the instant invention (see paragraphs 44-47 above). Hirai/Iyer also shows that the MgO layer is highly oriented (see, *e.g.*, col.3/ll.53-col.4/ll.12), but fails to disclose that this layer has a polycrystalline structure. Nonetheless, as admitted by the applicants (see, *e.g.*, spec./pp.7/ll19-20), highly oriented MgO layers are typically polycrystalline.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art that Hirai/Iyer's highly oriented MgO layer is polycrystalline since, as admitted by the applicants, highly oriented MgO layers are commonly polycrystalline.

Remarks

52. As taught by Auciello (US 5453661/col.5/ll.7-25), the highly oriented ferroelectric film of Hirai is polycrystalline.

53. As taught by Van Zant (pp.154-155), silicon dioxide layers are characterized by its passivating effect over the surface of a substrate.

Response to Arguments and Declaration under 37 CFR 1.132

54. The declaration under 37 CFR 1.132 filed in paper no. 15 on 7/28/2003 is insufficient to over the rejection of the claims upon the prior art made of record as set forth below.

55. The applicants argue:

The claimed invention is clearly different from Hirai. Hirai differently forms *first* the oriented buffer layer on the substrate and *then* the silicon oxide layer is formed by an anneal step in an oxygen ambient so as to be sandwiched between the substrate and the buffer layer. This resulted in a lower quality silicon oxide layer, which indicates that Hirai did not know how to form an oriented buffer layer on a non-crystalline surface.

The examiner responds:

Contradicting applicants' statement, Hirai clearly shows a process in which the silicon oxide layer is formed *first* and *then* the oriented buffer layer is formed on the oxide layer (see, *e.g.*, Hirai/col.7/ll.66-col.8/ll.10).

56. The applicants argue:

The process that Hirai uses to form the silicon oxide buffer is very different from the process of the instant invention. Therefore, the properties of the resulting interface between the silicon oxide and the silicon substrate are expected to be different. The nature of Hirai's silicon surface passivation cannot be the same as that of the present invention, which employs a thermal oxidation of a free silicon surface without any prior material deposited thereon.

The examiner responds:

Hirai clearly teaches (see, *e.g.*, col.7/ll.66-col.8/ll.10) to form a silicon oxide by thermal oxidation of a free silicon surface without any prior material deposited thereon. According to the applicants, since Hirai and the claimed invention use the same process to form a silicon oxide layer on a silicon surface, the passivating properties of Hirai's silicon oxide are expected to be the same as those of the claimed invention.

57. The applicants argue:

Hirai teaches an alternative sequence of steps wherein the silicon oxide layer is formed first and then an insulating buffer layer and a ferroelectric layer are formed. However, there is no disclosure in Hirai that he was aware that MgO has a tendency to grow self-oriented on an amorphous surface. Nor does he teach that he uses this special property of MgO in his invention.

The examiner responds:

Although the claims recite a step of forming an MgO layer having a highly-oriented structure on an oxide, the features upon which the applicants rely (*i.e.*, growing

an MgO layer on an amorphous surface, wherein the layer self-orients itself during the growing step so as to be highly-oriented) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

58. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

59. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

60. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

61. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/295, 438/3, 365/145	10/4/2003
Other Documentation: PLUS Analysis	9/11/2002
Electronic Database(s): EAST (USPAT, EPO, JPO)	10/4/2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800

Marcos D. Pizarro-Crespo
Patent Examiner
Art Unit 2814
703-308-6558
marcos.pizarro@uspto.gov

MDP/mdp
October 4, 2003